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(54) Coding and decoding system using crc check bit

(57) A coding and decoding system which uses CRC check bits is disclosed. When a coding apparatus performs coding, symbol interleaving is performed after coding by an outer code of a concatenated code, and coding by an inner code is performed after CRC check bits are added. Then, upon decoding by a decoding apparatus, error detection using the CRC check bits is performed after decoding of the inner code, and after symbol deinterleaving is performed, decoding of the outer code by erasure decoding or error correction is performed depending upon the number of symbols included in a frame in which an error has been detected.

Fig. 3a

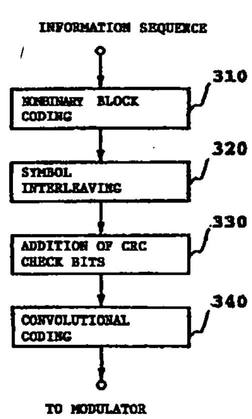
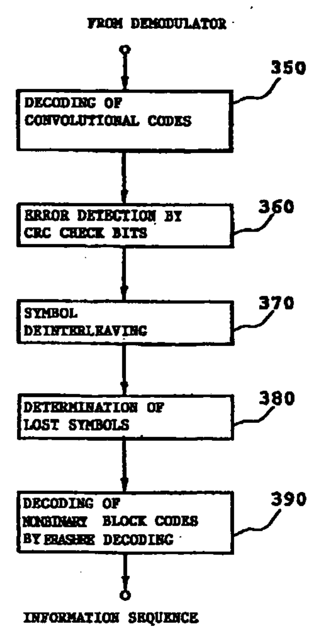


Fig. 3b



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Description

This invention relates to a coding and decoding system, and more particularly to a channel coding and decoding system for digital mobile communication.

Conventionally, when a coding and decoding system which includes a coding apparatus and a decoding apparatus, particularly a channel coding and decoding system which is used for digital mobile communication, is employed, channel coding is used in order to prevent a variation of the received power called fading or deterioration of the communication quality caused by interference from a user who uses the same frequency channel. From among various coding systems, a coding system which uses a convolutional code is frequently used, since a high error correction effect can be obtained even with a channel which exhibits a comparatively high bit error ratio (BER).

However, the coding system by a convolutional code sometimes gives rise to error in propagation from its characteristics. When only the coding system by a convolutional code is employed, occurrence of burst errors cannot be avoided when the received power is lowered significantly by fading or in a like case.

As one of methods for preventing burst errors, a method by interleaving which replaces an information sequence with respect to time is employed frequently. The method by interleaving signifies a method wherein, on the transmission side, an information sequence of a fixed amount is stored into a buffer and then rearranged in order, and on the reception side, the information sequence is rearranged to restore the original order thereof. Generally, as the interleave size, which is the size of the buffer, increases, the correction capacity of burst errors increases. However, there is a problem that, as the interleave size increases, delay which arises upon decoding increases.

As another one of methods for reducing burst errors, a coding method which employs a concatenated code is available. The coding method by a concatenated code is a method which first performs error correction coding for an information sequence and then performs further coding for the error corrected information sequence thereby to effect correction of burst errors efficiently. The coding performed first is called outer coding, and the coding performed second is called inner coding. In a concatenated code which is employed in order to reduce burst errors, a convolutional code is used for the inner code while a nonbinary block code wherein a block is partitioned into certain symbol units is used for the outer code. Here, one symbol is a unit of a fixed number of bits, and while 8 bits are frequently used. However, one symbol is not limited to 8 bits.

Figs. 1a and 1b are flow charts illustrating a conventional basic coding method by a concatenated code.

Fig. 1a is a flow chart illustrating processing on the transmission side, and nonbinary block coding is performed for an information sequence (step 110) and then convolutional coding is performed for a frame which is an information sequence thus produced (step 120). Conventionally, interleaving is sometimes performed after each coding in order to raise the error correction capacity, but this has not necessarily been essential.

Fig. 1b is a flow chart illustrating processing on the reception side, and decoding of convolutional codes is performed for a demodulated information sequence (step 130) and decoding of nonbinary block codes is performed for the decoded information sequence (step 140). In the nonbinary block codes, the number of error symbols which can be corrected in one frame is called error correction capability. Meanwhile, when the positions of error symbols are specified in one frame, the number of symbols whose errors can be corrected is called erasure decoding capability. The erasure decoding capability when decoding is performed using nonbinary block codes is equal to or higher than the error correction capability. Particularly when a code having a erasure decoding capability higher than the error correction capability is used as the outer code, decoding of a higher efficiency can be achieved by performing erasure decoding.

However, in order to effect erasure decoding, information for specifying the positions of error symbols is required. The SOVA (Soft Output Viterbi Algorithm) has been proposed which is a decoding system wherein, when convolutional codes are to be decoded using Viterbi decoding in an inner code, the reliability of decoded symbols is calculated, and then in decoding of the outer code, the reliability is utilized (J. Hagenauer and P. Hoeher, "A Viterbi Algorithm with Soft-Decision Outputs and its Applications", IEEE).

Fig. 2 is a flow chart illustrating decoding processing of the SOVA. In this system, in determining a survivor path in decoding of a convolutional code (step 210), reliability information 240 for each bit representing by what degree a path which has been determined as a survivor path is reliable is calculated based on a metric of the path and outputted together with decoding result 260. Then, symbol deinterleaving is performed based on reliability information 240 for each bit, and decoding result 270 and deinterleaved reliability information 250 for each bit are outputted (step 220). Finally, when performing decoding of nonbinary block codes which are outer codes, decoding of deinterleaved decoding result 270 is performed using deinterleaved reliability information 250 for each bit (step 230).

In decoding of inner codes, a large amount of calculation is required in order to calculate reliability information for each bit. Meanwhile, in decoding of outer codes, since the reliability information for each bit is utilized, a large storage capacity is required. Further, since the amount of reliability information transmitted from a decoding apparatus for an inner code to a decoding apparatus for an outer code is large, there is a problem that a channel having a large capacity is required between the decoding apparatus for an inner code and

the decoding apparatus for an outer code.

It is an object of the present invention to provide a coding and decoding system which effects erasure decoding effectively by a small amount of calculation and has a high error correction capability.

In order to attain the object described above, according to the present invention, when effecting channel coding using a concatenated code, a coding apparatus on the transmission side first adds CRC check bits after coding by outer codes and then performs coding by inner codes. Then, a decoding apparatus on the reception side performs error detection using the CRC check bits after decoding of the inner codes and performs symbol deinterleaving, and hereinafter it determines symbols to be erasure decoded using a result of the error detection and then performs decoding of the outer codes.

By the construction described above, when compared with an alternative case wherein channel coding is performed using a concatenated code by which decoding of outer codes is effected by performing error correction, error correction with a higher degree of accuracy can be achieved,

Further, according to the present invention, since it is required only to perform error correction with the CRC check bits after decoding of the inner codes is completed and output one bit representing whether or not a frame error has been detected to the decoder for an outer code, implementation of an apparatus is facilitated when compared with that by the SOVA and besides a characteristic similar to that of the SOVA can be obtained.

Further, according to the present invention, erasure decoding is performed only when all errors can be corrected by erasure decoding, but when no all errors can be corrected by erasure decoding, decoding is performed by error correction. Accordingly, the present invention can achieve more effective error correction than that of an alternative case wherein erasure decoding is not performed but only error correction is performed.

The above and other objects, features and advantages of the present invention will become apparent from the following description with reference to the accompanying drawings which illustrate examples of the present invention.

Figs. 1a and 1b are flow charts illustrating processing of a conventional basic coding method by a concatenated code;

Fig. 2 is a flow chart illustrating processing of the SOVA;

Fig. 3a is a flow chart illustrating coding of a first embodiment of the present invention, and Fig. 3b is a flow chart illustrating decoding of the first embodiment of the present invention;

Fig. 4 is a bit diagram in coding of the first embodiment of the present invention;

Fig. 5 is a bit diagram in decoding of the first embodiment of the present invention;

Fig. 6 is a flow chart illustrating decoding in a second embodiment of the present invention;

Fig. 7 is a bit diagram in decoding of the second embodiment of the present invention;

Fig. 8a is a block diagram showing a construction of a coding apparatus in a third embodiment of the present invention, and Fig. 8b is a block diagram showing a construction of a decoding apparatus in the third embodiment of the present invention; and

Fig. 9 is a diagram illustrating average bit error ratio characteristics of various decoding systems using a signal to noise power ratio as a parameter.

First Embodiment

First, coding processing is described with reference to Fig. 3a.

First, an information sequence to be transmitted is converted into a multiple information sequence, and nonbinary block coding wherein nonbinary block codes are used for the outer code of a concatenated code is performed for the resulting multiple information sequence (step 310). Then, symbol interleaving is performed for the information sequence to which check symbols are added (step 320). For the check symbols, for example, an RS code (Reed-Solomon Code) can be used. Then, the interleaved information sequence is converted back into binary information sequence and CRC (Cyclic Redundancy Code) check bits are added to the binary information sequence (step 330), and convolutional coding wherein a convolutional code is used for the inner code of a concatenated code is performed for the resulting binary information sequence (step 340). Then, a resulting signal sequence is outputted to a modulator.

Now, decoding processing is described with reference to Fig. 3b.

First, decoding of convolutional codes which are inner codes of a concatenated code is performed for an information sequence produced by decoding of a received signal sequence (step 350). Error detection by CRC check bits is performed for the decoded information sequence (step 360), and symbol deinterleaving is performed for a result of the decoding and a result of the error detection (step 370) to produce frames of nonbinary block codes which are outer codes of the concatenated code. Then, symbols which have been included in those frames from which errors have been detected based on the interleaved decoding result and error detection result are regarded and determined as lost symbols (step 380). When an RS code is used for the check symbols, error correction is performed regarding that the symbols other than the symbols which are regarded as having been lost have no error, and decoding of nonbinary block codes by erasure decoding is performed (step 390). Finally, the information is con-

verted into binary information and outputted as an information sequence of a decoding result.

Fig. 4 is a view showing a bit diagram of the coding apparatus of the first embodiment of the present invention. In Fig. 4, corresponding elements to those of Fig. 3a are denoted by same reference symbols.

First, information sequence 510 to be transmitted is partitioned into block units and stored into a buffer (step 520). Here, the buffer size, that is, the interleave size, is a product of one block length of nonbinary block codes and the depth of the interleave. While it is illustratively shown in FIG. 4 that the depth of the interleave is 4, this number is a mere value for convenience of explanation.

Then, each block is partitioned into symbol units and conversion of the information sequence into a multiple information sequence is performed (step 530). As described above, one symbol signifies a unit of a fixed number of bits, and while 8 bits are frequently used, one symbol is not limited to 8 bits. One block partitioned in symbol units is called one frame. While, in the figure (step 530) of the conversion of the information sequence into a multiple information sequence, four frames are illustratively shown in four different patterns, this illustration is intended to make description of the symbol interleaving (step 320) clear. In contrast, the pattern of information sequence 510 indicates that the information sequence is binary information.

Then, the information sequence after the multiple conversion is converted into multiple blocks and check symbols 540 are added to the multiple blocks (step 310). Thereafter, symbol interleaving is performed (step 320), and then the information sequence is converted back into a binary information sequence (step 550). Then, CRC check bits 560 are added (step 330). Finally, convolutional coding is performed as inner codes of a concatenated code (step 340), and resulting convolutional codes are outputted to the transmitter.

Fig. 5 is a view showing a bit diagram of a decoding apparatus of the first embodiment of the present invention. In Fig. 5, corresponding elements to those of Fig. 3b are denoted by same reference symbols.

First, signal 630 obtained by decoding a received signal is partitioned into block units and stored into a buffer (step 640). Then, coding of convolutional codes is performed (step 350). Here, each location painted black indicates a position of a bit with which an error in decoding has occurred. Then, CRC check bits 650 are added to a result of decoding obtained by decoding of the convolutional codes.

Thereafter, error detection by CRC check bits 650 is performed (step 360). Each block in which a decoding error has been detected by the error detection is indicated as CRC NG, but each block in which no decoding error has been detected is indicated as CRC OK. Then, multiple conversion of the information sequence is performed (step 610), and each of symbols included in frames in which errors have been detected is indicated by a pattern with slanting lines added thereto. Furthermore, even after symbol deinterleaving is performed, the symbol is indicated by the same pattern (step 370). Here, check symbols 660 are added to the symbol deinterleaved decoding result.

Then, the symbols having the patterns added thereto are regarded as symbols which have been lost in determination of lost symbols. Each of the symbols regarded as lost symbols is indicated by mark X (step 380). Then, decoding of the nonbinary block codes by erasure decoding (step 390) is performed. Finally, the information is converted into binary information (step 620) and outputted as information sequence 670 of the decoding result.

Second Embodiment

Fig. 6 is a flow chart illustrating a second embodiment of the present invention.

Referring to Fig. 6, decoding of convolutional codes (step 350), error detection by CRC check bits (step 360), symbol deinterleaving (step 370) and determination of lost symbols (step 380) are similar to those of Fig. 3b.

Then, after the determination of lost symbols (step 380), it is discriminated whether or not the number of symbols included in each of the frames in which errors have been detected is higher than the erasure decoding capability of the outer code (step 460), and if the number of symbols is not higher, then decoding of multiple blocks by erasure decoding (step 420) is performed, regarding symbols which have been included in each of those frames in which errors have been detected as lost symbols, by error correction using, for example, an RS code as in the case of the first embodiment described above. If the number of symbols included in a frame in which an error has been detected is higher than the erasure decoding capability of the outer code, it is impossible to correct all of the errors by erasure decoding.

However, where the number of error detected symbols in a frame is not higher than the error correction capability, since all errors can be corrected, for example, by error correction which utilizes an RS code, erasure decoding is not performed, but only error correction is performed (step 430).

Since the accuracy in error correction by CRC check bits is very high, a result of detection of frame errors can be regarded as almost correct. Therefore, in the present embodiment, erasure decoding is performed only when all errors can be corrected by erasure decoding, but when not all of errors can be corrected by erasure decoding, decoding is performed by error correction.

Fig. 7 is a view showing a bit diagram of the present embodiment. In Fig. 7, corresponding elements to those of Fig. 6 are denoted by same reference symbols.

First, signal 800 obtained by decoding a received signal is partitioned into block units and stored into the

buffer (step 790). Thereafter, decoding of convolutional codes is performed (step 410). In the decoding of convolutional codes, the position of each bit with which a decoding error has occurred is indicated by two blocks painted black. Then, in error detection (step 420) by CRC check bits, two blocks with which decoding errors have occurred are indicated as CRC NG. In multiple conversion of the information sequence (step710), symbols in the two frames in which errors have been detected are indicated by a pattern with slanting lines, and also in a symbol deinterleaved decoding result (step 430), such symbols are indicated by a similar pattern. To the symbol deinterleaved decoding result, check symbols 760 are added as seen in Fig. 7.

In Fig. 7, it is illustratively shown that the number of symbols included in two frames in which errors have been detected is higher than the erasure decoding capability. Accordingly, no erasure decoding is performed (step 720), but only decoding of nonbinary block codes by error correction is performed (step 730). Finally, the information is converted into binary information (step 740) and outputted as information sequence 750 of the decoding result.

Third Embodiment

Fig. 8a is a block diagram showing a construction of a coding apparatus of a channel coding and decoding system of a third embodiment of the present invention, and Fig. 8b is a block diagram showing a construction of a decoding apparatus.

Also in the present embodiment, the coding apparatus employs an RS code for the outer code of a concatenated code for an information sequence. In the decoding apparatus, erasure decoding symbols are determined by error detection by CRC check bits, and symbol interleaving is performed and decoding is performed by error correction by an RS code. Accordingly, the present embodiment can achieve more effective error correction than an alternative case wherein erasure decoding is not performed but only error correction by an RS code is performed.

The coding apparatus of the present embodiment includes multiple converter 900 for multiple converting of an information symbol, RS encoder 915 for encoding of an RS code which is the outer code of a concatenated code, symbol interleaver 920, CRC check bit adder 925, convolutional encoder 930 for encoding of a convolutional code which is the inner code of a concatenated code, bit interleaver 935, and modulator 940.

The decoding apparatus includes demodulator 950, bit deinterleaver 955, convolutional code decoder 960, error detector 965 for detecting by CRC check bits, symbol deinterleaver 970, RS code decoder 975 for decoding by erasure decoding, RS code decoder 980 for decoding by error correction, and binary converter 990 for converting information to a binary information.

Next, operation of the present apparatus is described. First, a binary information sequence to be transmitted is inputted to multiple converter 900. By multiple converter 900, a plurality of information bits are converted into one symbol. To the information sequence after conversion into multiple symbols, check symbols are added by RS encoder 915, and symbol interleaving is performed by symbol interleaver 920. Thereafter, the information is converted into binary information, and CRC check bits calculated by CRC check bit adder 925 are added to the binary information. Then, convolutional coding is performed for the binary information sequence by convolutional encoder 930, and then, bit interleaving is performed by bit interleaver 935, and hereinafter the resulting information is outputted to modulator 940. The information sequence is modulated by modulator 940 and sent to a radio transmitter.

In the decoding apparatus, a signal sequence transmitted thereto from a radio receiver is first demodulated by demodulator 950, and interleaving is performed for the signal sequence by bit deinterleaver 955, and hereinafter decoding of inner codes is performed by convolutional code decoder 960. Thereafter, detection of frame errors is performed by error detector 965, and the information is converted into multiple information. Then, the multiple information sequence undergoes deinterleaving by symbol deinterleaver 970. Then, for each frame, if the number of symbols which include errors is within the range of erasure decoding, erasure decoding is performed by RS code decoder 975 for erasure decoding, but if the number of symbols which include errors is outside the range of erasure decoding, error correction is performed by RS code decoder 980 for error correction. Finally, the information is converted back into binary information by binary converter 990 to obtain a received sequence.

Bit interleaver 935 and bit deinterleaver 955 in the present embodiment are added in order to raise the error detection and correction capabilities. Accordingly, a bit interleaver and a bit deinterleaver can be added similarly also to the other embodiments of the present invention.

Fig. 9 illustrates bit error radio characteristics of an inner code, an inner code + an outer code in which error correction is performed, an inner code + an outer code for which the SOVA is used, and an inner code + an outer code which employs CRC check bits in the present embodiment where a signal to noise power ratio is used as a parameter. The axis of ordinate represents the average bit error ratio (average BER), and the axis of abscissa represents the signal energy to thermal noise power spectral density ratio (Eb/No). When compared with decoding which only involves error correction, the systems of the SOVA and the present embodiment which make use of reliability information for each bit in decoding of the inner code exhibit an improvement by approximately 1 dB in Eb/No where the average bit error ratio is 1.0×10^{-5}.

While the SOVA requires, upon decoding, calcula-

tion of a reliability degree for each bit and outputting of a result of the decoding for each bit to the outer code, with the first to third embodiments described above, it is required only to perform error correction by CRC check bits after decoding of the inner code is completed and output one bit representing whether or not a frame error has been detected to the decoder for an outer code. Accordingly, when compared with the SOVA, implementation of an apparatus is facilitated, and a characteristic similar to that of the SOVA can be obtained.

While preferred embodiments of the present invention have been described using specific terms, such description is for illustrative purposes only, and it is to be understood that changes and variations may be made without departing from the spirit or scope of the following claims.

Claims

1. A coding method, comprising the steps of:

   performing multiple conversion wherein a block of an information sequence is partitioned into symbols of a fixed number of bits to make frames;
   performing coding by an outer code for the frame units;
   performing interleaving in units of a symbol for the frames for which the coding by an outer code has been performed;
   adding a check bit in units of a block to the frames for which the interleaving in units of a symbol has been performed; and
   performing coding by an inner code for the information sequence to which the check bits have been added.

2. A decoding method, comprising the steps of:

   decoding an information sequence for which coding by an inner code has been performed;
   performing error detection in units of a block with detection bits added thereto;
   performing multiple conversion wherein each block after the error detection in units of a block has been performed is partitioned into symbols of a fixed number of bits to produce frames;
   performing interleaving for the frames; and
   performing decoding of an outer code by erasure decoding.

3. A decoding method as claimed in claim 2, wherein the step of performing decoding of an outer code includes the step of performing, if the number of symbols included in the frames after the deinterleaving, in which errors have been detected, is not larger than the number of symbols which can be corrected by erasure decoding, decoding of the outer code by erasure decoding, but performing, if the number of symbols included in the frames after the deinterleaving, in which errors have been detected, is larger than the number of symbols which can be corrected by erasure decoding, decoding of the outer code by error correction.

4. A coding and decoding method, comprising:

   a coding method as claimed in claim 1; and
   a decoding method as claimed in claim 2 or 3.

5. A method as claimed in claim 1, 2,3 or 4, wherein the information sequence is an information sequence in digital mobile communication.

6. A method as claimed in any one of claims 1 to 5, which is used as a channel coding method or channel decoding method, respectively.

7. A coding apparatus, comprising:

   multiple conversion means for performing multiple conversion wherein a block of an information sequence is partitioned into symbols of a fixed number of bits to make frames;
   outer code coding means for performing coding by an outer code for the frame units;
   symbol interleaving means for performing interleaving in units of a symbol for the frames for which the coding by an outer code has been performed;
   check bit addition means for adding a check bit in units of a block to the frames for which the interleaving in units of a symbol has been performed; and
   inner code coding means for performing coding by an inner code for the information sequence to which the check bits have been added.

8. A decoding apparatus, comprising:

   inner code decoding means for decoding an information sequence for which coding by an inner code has been performed;
   block error detection means for performing error detection in units of a block with detection bits added thereto;
   multiple conversion means for partitioning each block after the error detection by said block error detection means into symbols of a fixed number of bits to produce frames;
   deinterleaving means for performing interleaving for the frames; and
   outer code decoding means for performing decoding of an outer code by erasure decoding.

9. A decoding apparatus as claimed in claim 8, wherein said outer code decoding means includes means for performing, if the number of symbols included in the frames after the deinterleaving, in which errors have been detected, is not larger than the number of symbols which can be corrected by erasure decoding, decoding of the outer code by erasure decoding, but performing, if the number of symbols included in the frames after the deinterleaving, in which errors have been detected, is larger than the number of symbols which can be corrected by erasure decoding, decoding of the outer code by error correction.

10. An apparatus as claimed in claim 7, 8 or 9, wherein the information sequence is an information sequence in digital mobile communication.

11. An apparatus as claimed in claim 7, 8, 9 or 10, which is used as a channel coding apparatus, or a channel decoding apparatus, respectively.

12. A coding and decoding system, comprising: a coding apparatus as claimed in claim 7 or in claims 10 or 11 as dependent on claim 7; and a decoding apparatus as claimed in claim 8 or 9 or in claims 10 or 11 as dependent on claim 8 or 9.

Fig. 1a

PRIOR ART

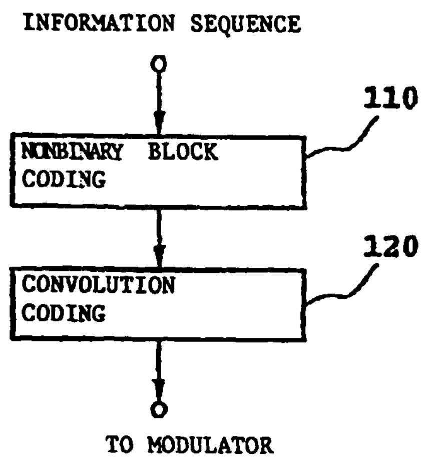


Fig. 1b

PRIOR ART

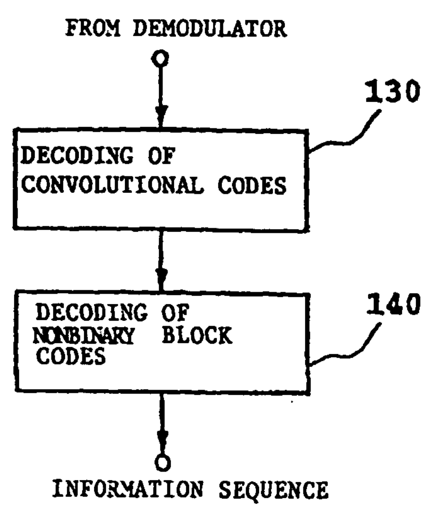


Fig. 2

PRIOR ART

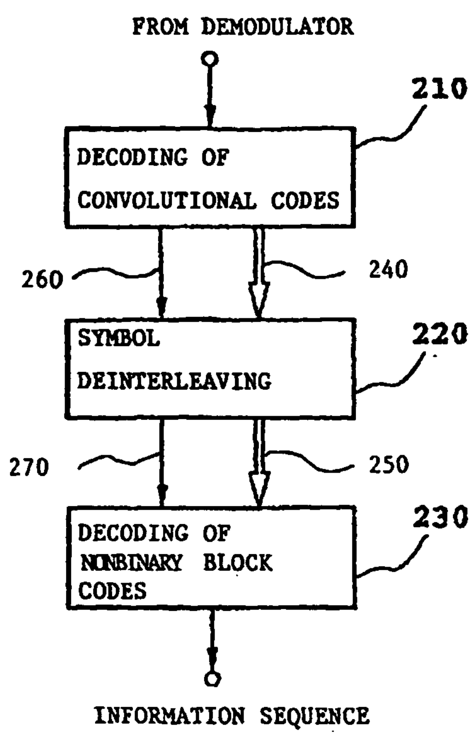


Fig. 3a

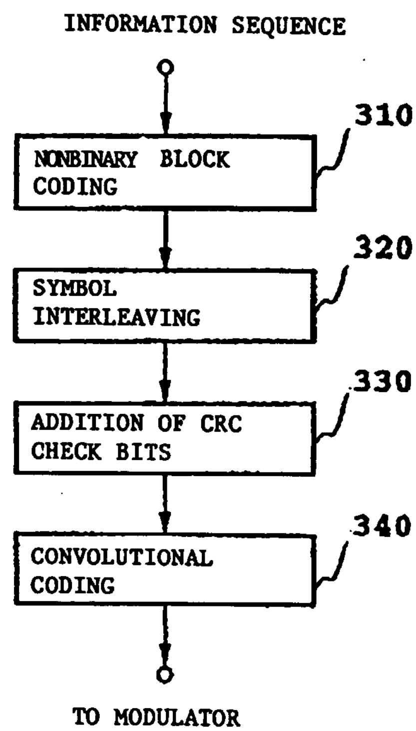

INFORMATION SEQUENCE
NONBINARY BLOCK CODING
310
SYMBOL INTERLEAVING
320
ADDITION OF CRC CHECK BITS
330
CONVOLUTIONAL CODING
340
TO MODULATOR

Fig. 3b

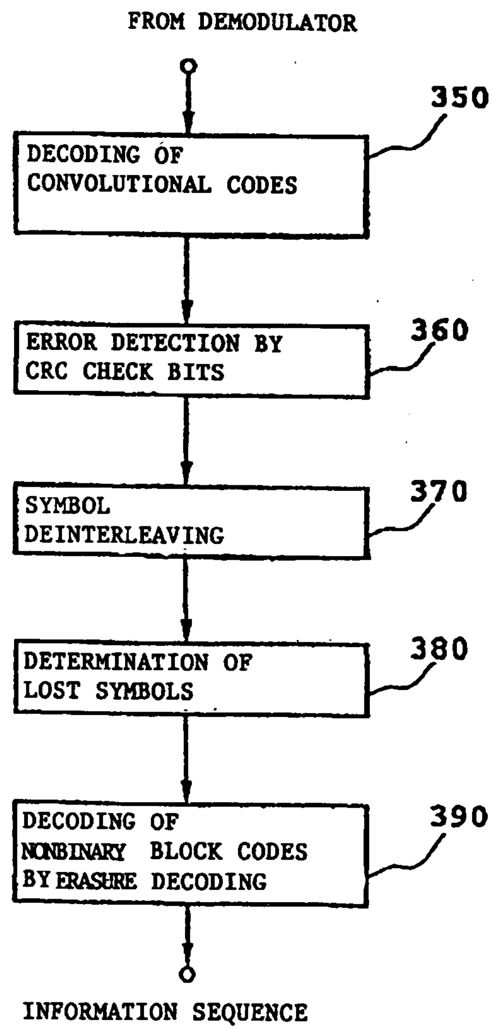

FROM DEMODULATOR
DECODING OF CONVOLUTIONAL CODES
350
ERROR DETECTION BY CRC CHECK BITS
360
SYMBOL DEINTERLEAVING
370
DETERMINATION OF LOST SYMBOLS
380
DECODING OF NONBINARY BLOCK CODES BY ERASURE DECODING
390
INFORMATION SEQUENCE

Fig. 4

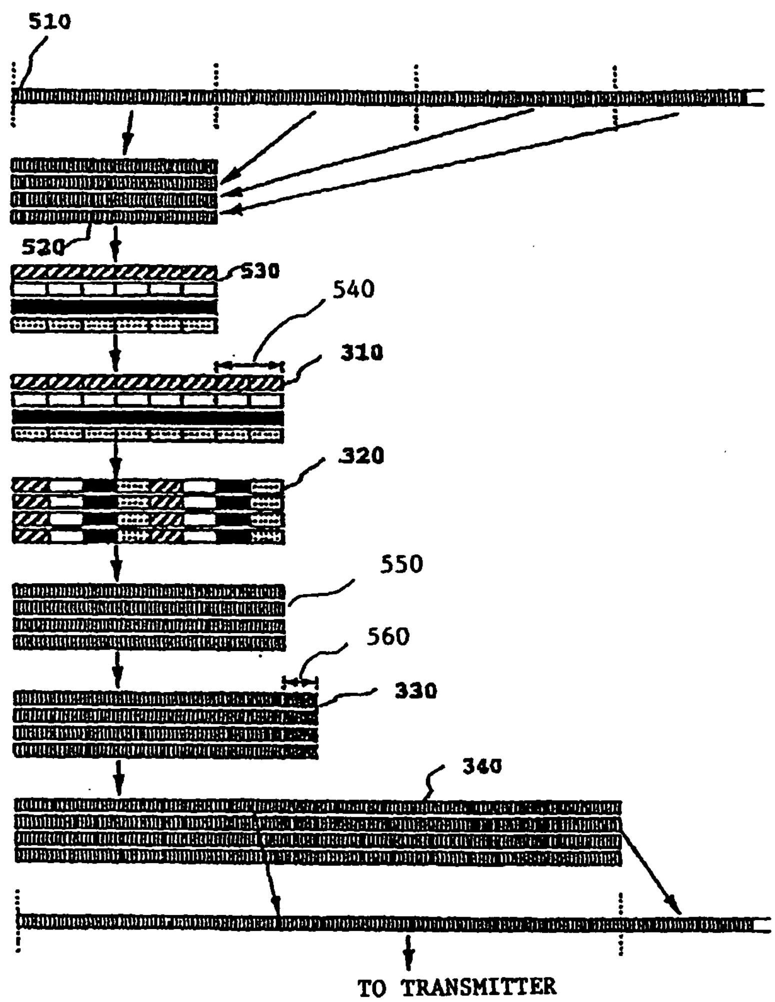


Fig. 5

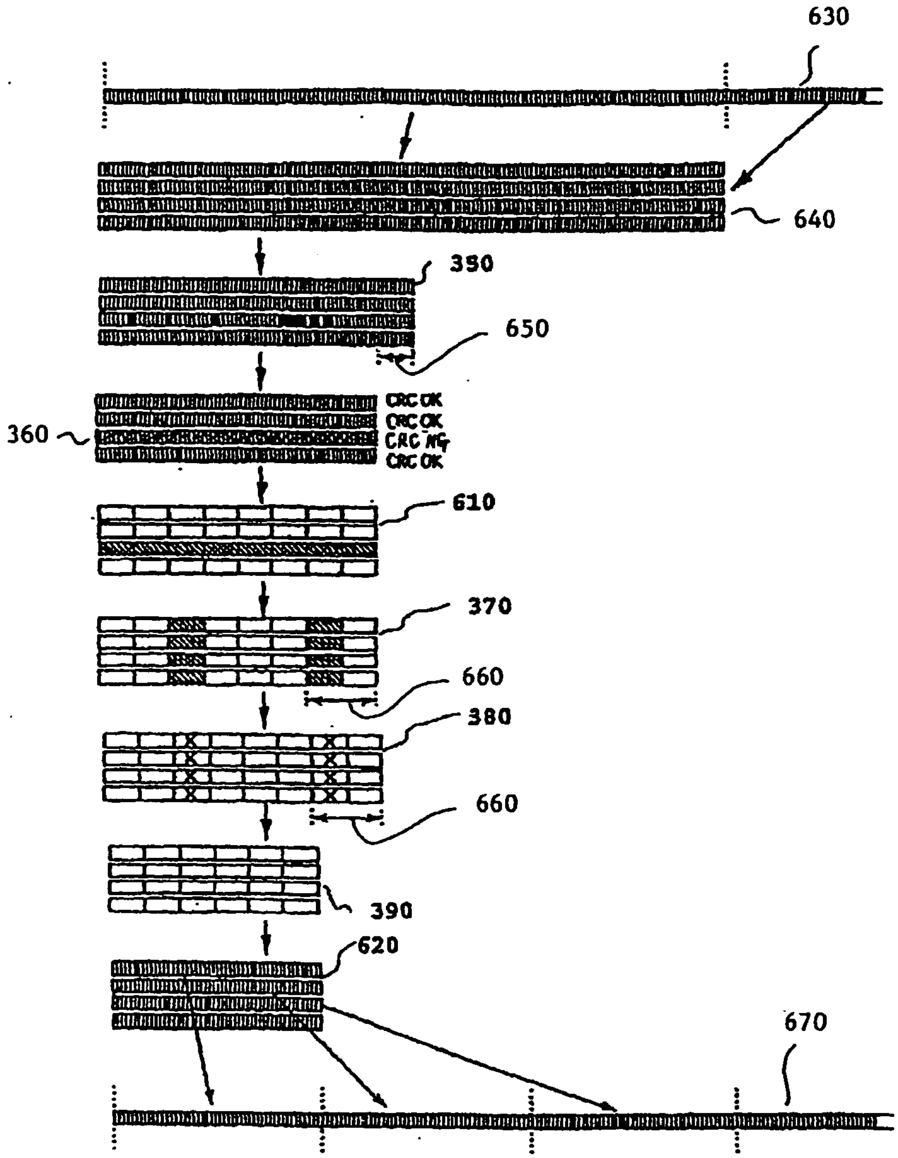

630
640
350
650
CRC OK
CRC OK
CRC NG
CRC OK
360
610
370
660
380
660
390
620
670

Fig. 6

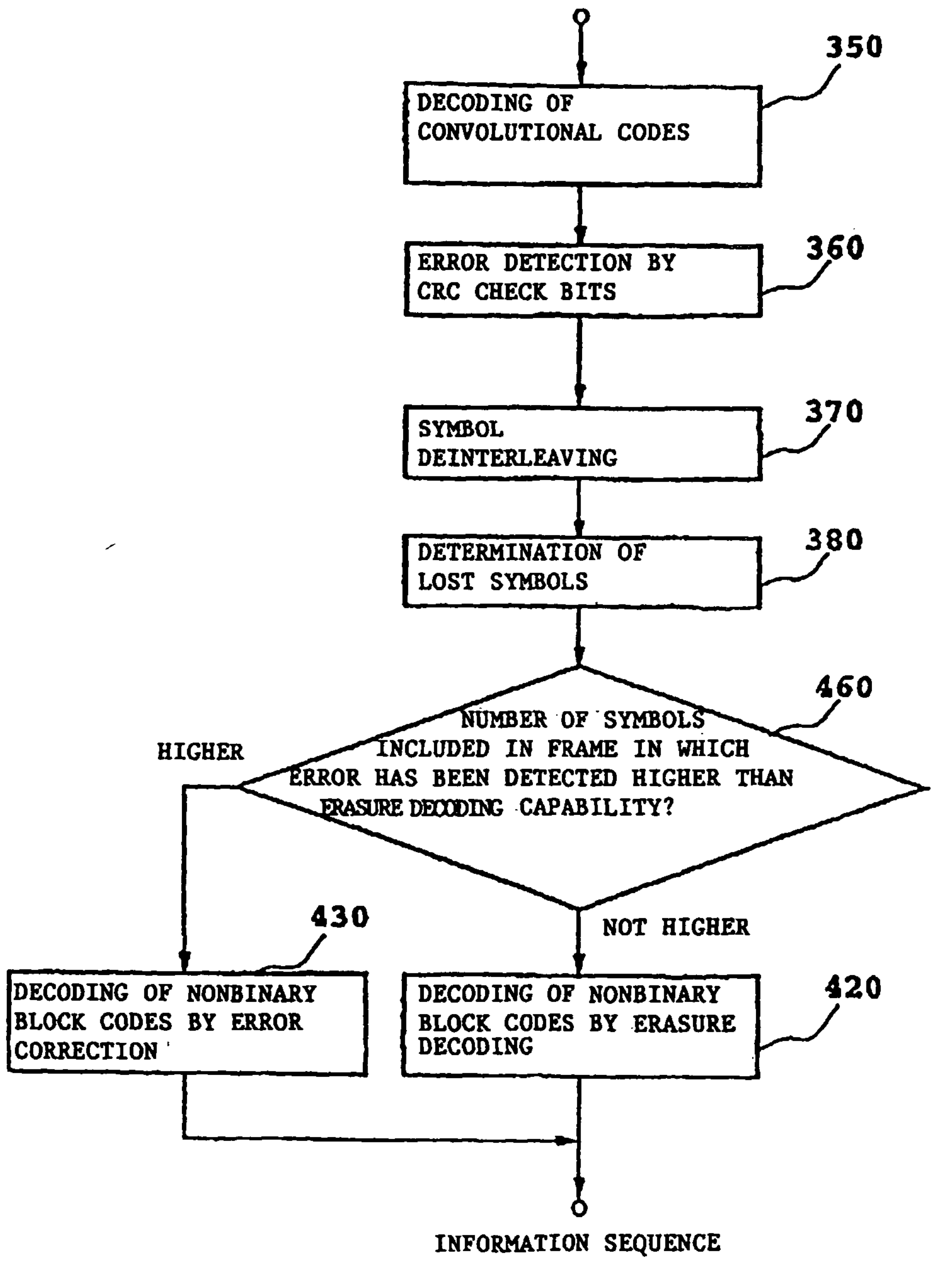
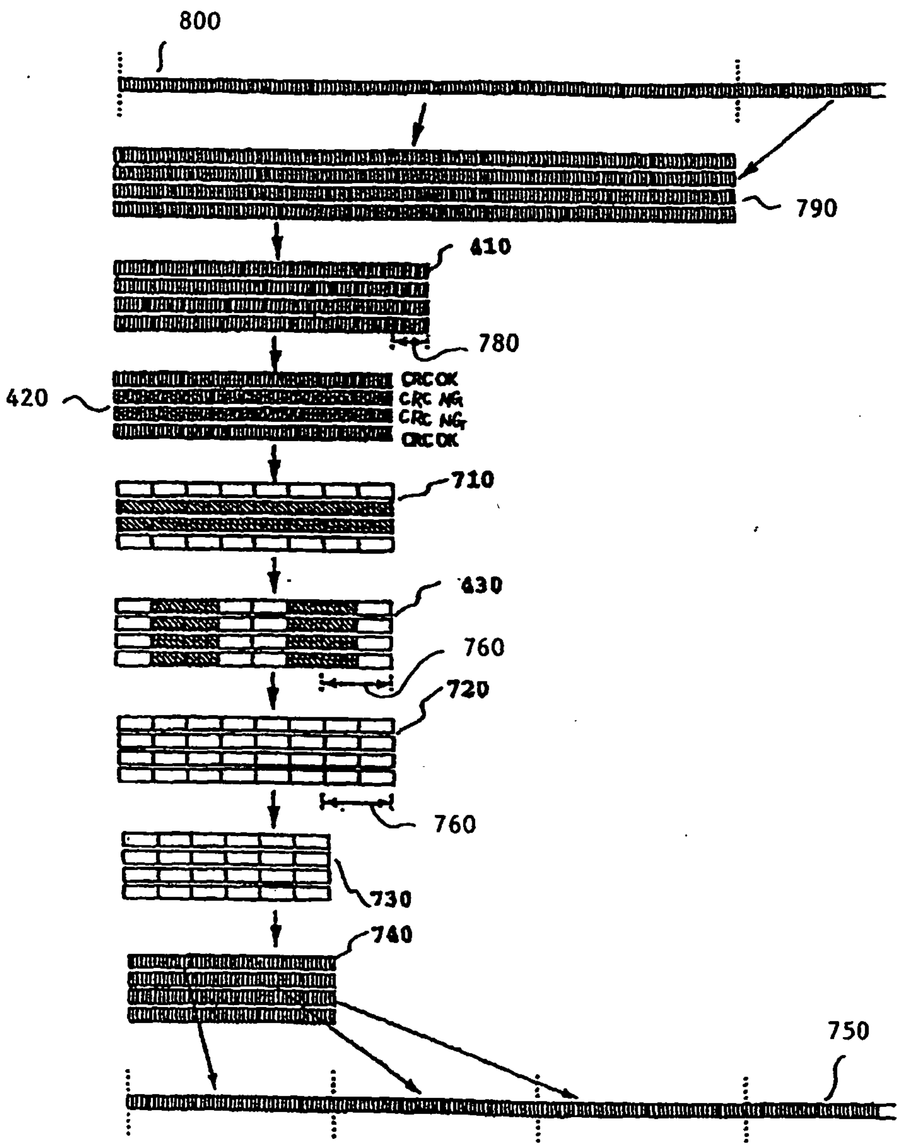

350
DECODING OF CONVOLUTIONAL CODES
360
ERROR DETECTION BY CRC CHECK BITS
370
SYMBOL DEINTERLEAVING
380
DETERMINATION OF LOST SYMBOLS
460
NUMBER OF SYMBOLS INCLUDED IN FRAME IN WHICH ERROR HAS BEEN DETECTED HIGHER THAN ERASURE DECODING CAPABILITY?
HIGHER
NOT HIGHER
430
DECODING OF NONBINARY BLOCK CODES BY ERROR CORRECTION
420
DECODING OF NONBINARY BLOCK CODES BY ERASURE DECODING
INFORMATION SEQUENCE

Fig. 7


800
790
410
780
420
CRC OK
CRC NG
CRC NG
CRC OK
710
430
760
720
760
730
740
750

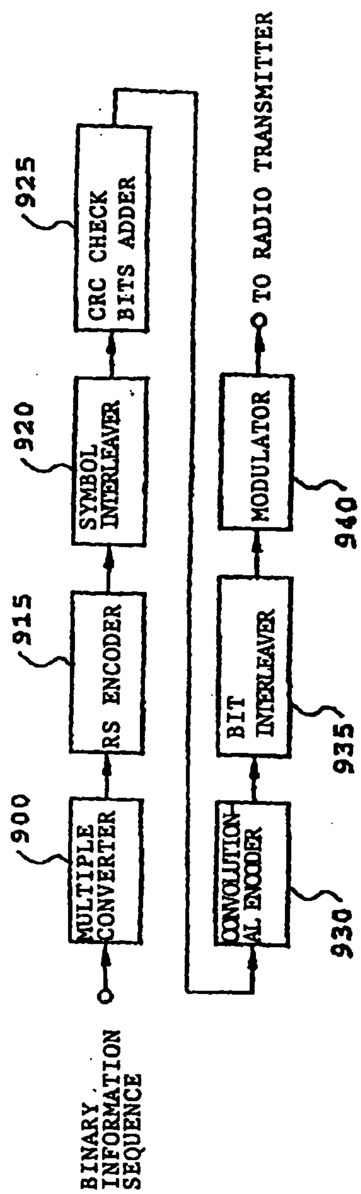

BINARY INFORMATION SEQUENCE
900 MULTIPLE CONVERTER
915 RS ENCODER
920 SYMBOL INTERLEAVER
925 CRC CHECK BITS ADDER
930 CONVOLUTIONAL ENCODER
935 BIT INTERLEAVER
940 MODULATOR
TO RADIO TRANSMITTER

Fig. 8a

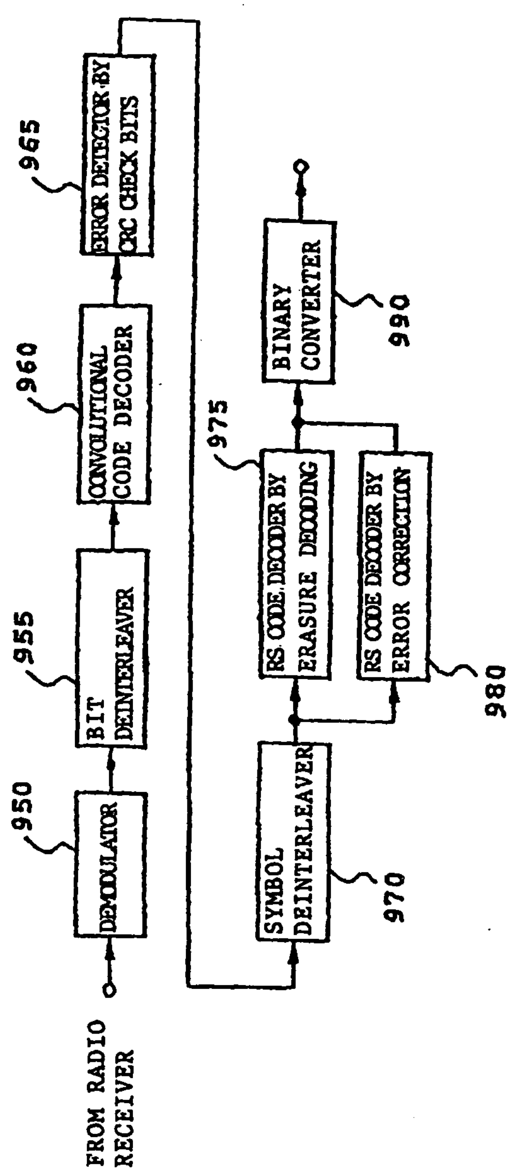
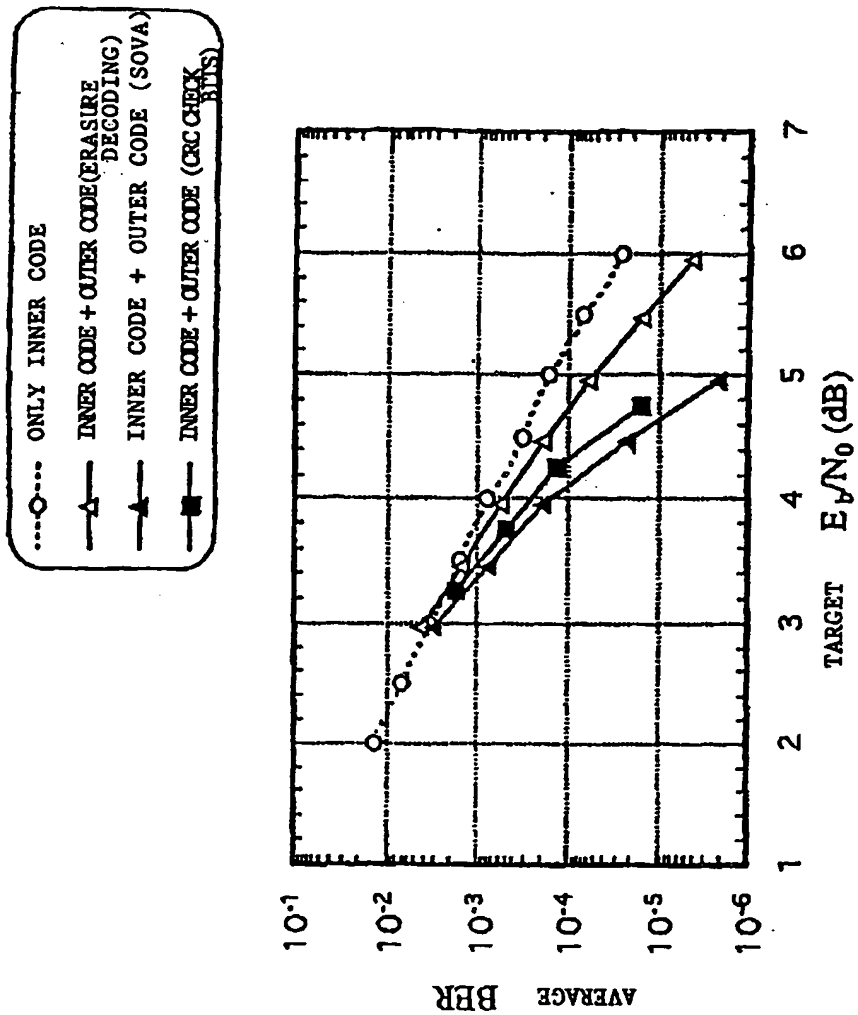

FROM RADIO RECEIVER
950 DEMODULATOR
955 BIT DEINTERLEAVER
960 CONVOLUTIONAL CODE DECODER
965 ERROR DETECTOR BY CRC CHECK BITS
970 SYMBOL DEINTERLEAVER
975 RS CODE DECODER BY ERASURE DECODING
980 RS CODE DECODER BY ERROR CORRECTION
990 BINARY CONVERTER

Fig. 8b

Fig. 9


ONLY INNER CODE
INNER CODE + OUTER CODE (ERASURE DECODING)
INNER CODE + OUTER CODE (SOVA)
INNER CODE + OUTER CODE (CRC CHECK BITS)
AVERAGE BER
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
1
2
3
4
5
6
7
TARGET E_b/N_0 (dB)